DE LA RECHERCHE À L'INDUSTRIE

cea

Project of a new readout chip

eRD6 meeting 19/04/2021

Introduction

Draft chip specifications

Prospects

www.cea.fr

INTRODUCTION

Common initiative of Sao Paulo Universities and CEA Saclay IRFU

- Large amount of competences on front-end, digitization, and digital treatments
- Sao Paulo Universities designed the SAMPA chip (readout chip for ALICE TPC)
- IRFU developed several front-end chips (AFTER, AGET, DREAM,...) and other kinds of chips (SAMPIC TDC,..)

Purpose of the project

- In the framework of the EIC project → compatible with streaming readout DAQ
- But meant to be versatile
- Primary goal: readout chip dedicated to most kinds of MPGD detectors
- Optionally, extension to other kinds of detectors (calorimeters ? photon detectors ?) and/or specific constraints (ps-level time resolution)

Present status

- Definition of the specification list in progress
- Preliminary studies on possible architecture, bloc structures, and possible technologies
- Choice of die production technology to be done (130nm ? 65nm ?)

DRAFT SPECIFICATION AND QUESTIONS

Front-end characteristics

- Number of channels: 32 or 64
- Peaking time range: 50 to 200 ns
- Rather large amplitude range: 75 fC to a few pC
- Max input capacitance: 200 pF
- Reversible polarity

Questions about the front-end specification

- Required dynamics, low vs large amplitude signals ?
- Peaking time range large enough ? Digital shaping should be considered ?
- Maximum input capacitance expected ?
- Time to recover from saturation ? (for instance after sparks)
- Internal discriminator ? (to generate trigger signals or for precise TDC measurement)
- Expected hit rates per channel (15 kHz ? 50 kHz ?), average and peak ? Amount of charges per unit of time from the detectors ? Also important for digital part

DRAFT SPECIFICATION AND QUESTIONS

Digitization

- ADC sampling frequency range: 10 to 40 MHz
- Dynamics: 12 bits
- Synchronization with external clock (internal PLL if necessary) + common timestamp reset signal or upstream heartbeat packets
- Optionally: additional TDC for time resolution better than 1 ns

Questions

- Larger sampling range required ? (lower rate to decrease data flow, or higher rate for short peaking time and better time resolution)
- 12-bits dynamics (0-4000) large enough ?
- What are the constraints about time resolution ?

DRAFT SPECIFICATION AND QUESTIONS

Data treatment and transfer

- Basic treatments: pedestal subtraction, common mode correction, zero suppression
- Optional advanced treatments: clusterization, time extraction, energy computation, etc…
- Optional possibility to customize data treatment
- Both streaming readout and trigger modes possible → external trigger input
- Possibility to emit trigger from digital processing
- Output buffer to store data before transfer (+ circular buffer in triggered mode)
- Max data flux to be defined → number of 1Gb/s links

Questions

- What data treatment is necessary beside zero suppression ? What about customization ?
- Expected data flux ? For instance 12bits x 25MHz x 64 channels = 23.5Gb/s
- Internal data storage ?
- Link speed: 1 Gb/s ? More ? How many links ? Buffer size ?

DRAFT SPECIFICATION AND QUESTIONS

Data flux

Streaming readout with Zero suppression

Hit rate kHz	Multiplicity	Hit word bit	Nb of words	Nb of channels	Chan BW Mb/s	ASIC BW Gb/s
25	4	32	3	64	2.4	0.6
50					4.8	1.23
15		16	10		3	0.77
25					5	1.28

Triggered readout without Zero suppression

Trigger rate kHz		Hit word bit	Nb of words	Nb of channels	Chan BW Mb/s	ASIC BW Gb/s
100		16	10	64	16	1
1000					160	10

DRAFT SPECIFICATION AND QUESTIONS

General specifications and environment

- Die/package size to be defined, small die size expected, at the level of 1 cm^2, depending on the complexity of the implementation
- Technology (130 or 65nm) to be defined, complex issue depending on several internal and external parameters
- Power consumption expected to be around 10-15 mW/ch, also depending on the environment constraints

Questions

- What are the expectation about the environment ? Temperature ? Max radiation level ?
- Constraints on the chip size ?

PROSPECTS

Chip definition in progress

- Draft specification
- Studies in progress on the possible chip architecture and elements
- Several questions still open

Collaboration around the chip

- Common initiative of Sao Paulo Universities and CEA Saclay
- Still informal, formalization in progress
- Not funded yet
- Other contributors are welcome !